

Serial No. 10/533,062
Amendment
Responsive to Office Action dated October 9, 2007

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REMARKS**Pending Claims**

Claims 1-4, and 6 are pending. Claims 5 and 7 have been canceled without prejudice or disclaimer. Claims 1 and 6 have been amended. No new matter has been added.

Information Disclosure Statement

The Examiner has not considered three of the literature documents listed in the IDS (AR, AS & AU of the Form PTO-1449) filed April 28, 2005. As soon as copies of these documents and English language equivalents are received from the applicant, they will be submitted to obtain the Examiner's consideration.

Claim Rejections Under 35 U.S.C. §102 and §103

Claims 1 and 7 are rejected under 35 U.S.C. §102(e) as being anticipated by Flake et al, U.S. Patent No. 7,035,781 (Flake) and/or Bowen, U.S. Patent No. 6,691,301. Further, claims 2-5 and 7 are rejected under 35 U.S.C. §103(a) as being unpatentable over Flake et al and/or Bowen, in view of Hines, U.S. Patent Publication No. 2005/0246682. Applicants request reconsideration of the rejections in view of the foregoing amendments and for the following reasons.

Claim 1 is directed to a system development method of the invention and independent claim 6 is directed to a data processing system of the invention. Each of claims 1 and 6 has been amended to set forth that the program descriptions define a plurality of devices by

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employing a Java program language capable of describing parallel operations. Further, the claims have been amended to state that the program descriptions define the devices on a single bus by using a run method of the Java program language and define clock synchronizations of the device by using barrier synchronizations. According to the amended claims, program codes which are to be executed in a thread constituting a multi-thread are described in the run method.

Support for the amendments to claims 1 and 6 is provided in the Specification. In particular, see page 13, lines 1-13, which describes a design method shown in Figure 1. In particular, the model of the system to-be-designed is designed by descriptions based on the Java language, according to the Specification. Each device is on a single bus and is described using the run method of the Java language. Further, program codes which are to be executed in a thread constituting a multi-thread are described in the run method. Also, the Specification sets forth that a clock is expressed using barrier synchronization, which is explained as being a synchronization technique for waiting for all data which ought to be processed at the same time, in the case of receiving data from a plurality of modules.

As amended, the claims are patentable over Flake and Bowen, whether or not further considered in view of Hines. Flake is directed to a mixed language simulator which blends one or more hardware description languages (HDL) with one or more conventional programming languages in an integrated programming environment. See column 3, lines 61-65 of the reference. However, Flake does not disclose or suggest providing program descriptions which define a plurality of devices by employing a Java program language capable of describing parallel operations, as claimed by applicants. Accordingly, Flake does

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not anticipate claims 1 and 6 under 35 U.S.C. §102(e).

Bowen describes a development tool which uses Field Programmable Gate Arrays (FPGAs) which are logic circuits that can be repeatedly reconfigured in different ways.

Bowen discloses that the preferred programming language used is Handel-C as a high-level language to program the FPGAs. See column 9, lines 55-65 of the reference. Accordingly, Bowen does not disclose or suggest the claimed combination of amended claims 1 and 6. Therefore, the rejection under 35 U.S.C. §102(e) should be withdrawn.

In the rejection under 35 U.S.C. §103(a), Hines has been relied upon for disclosing programming languages. For example, in the Background of the Invention section of the application, Hines mentions object-oriented programming languages. However, Hines is directed to a system and method for debugging concurrent software systems. According to the invention of the amended claims, however, the program descriptions are defined by a plurality of devices by employing a Java program language capable of describing parallel operations and program descriptions define the devices on a single bus by using a run method of the Java program language, and further define clock synchronizations of the device by using barrier synchronizations. As amended, the independent claims further set forth that in the run method, program codes which are to be executed in a thread constituting a multi thread are described. Hines does not disclose or suggest these aspects of the invention as claimed, and therefore the combination of Flake and/or Bowen with Hines does not render the invention as now claimed unpatentable under 35 U.S.C. §103(a). Accordingly, the rejection should be withdrawn and claims 1-4 and 6 should be allowed.

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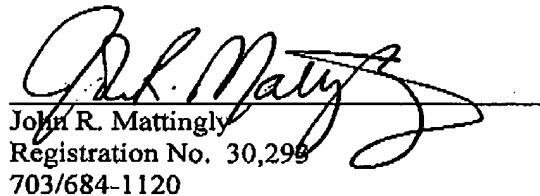
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Conclusion

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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